MT6339N5

60V/10A Complementary Enhancement Mode Field Effect Transistor

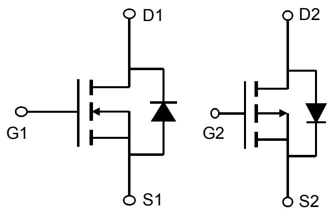
MT Semiconductor®

http://www.mtsemi.com

General Description

The MT6339N5 uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used in H-bridge, Inverters and other applications.

Simplified Schematic



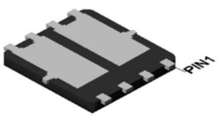
Features

N-channel	P-channel
V_{DS} (V) = 60V	-60V
I_D = 10A (V_{GS}=10V)	-10A (V_{GS} = -10V)
$R_{DS(ON)}$	$R_{DS(ON)}$
=35m Ω (V_{GS}=10V)	=64mΩ (V_{GS} = -10V)
=40m Ω (V_{GS}=4.5V)	=75mΩ (V_{GS} = -4.5V)

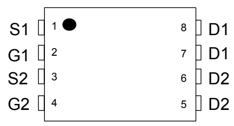
100% Rg tested

MARKING DIAGRAM & PIN ASSIGNMENT

DFN5X6-8L



Top View



Absolute Maximum Ratings T_A=25°C unless otherwise noted					
Parameter		**Symbol**	**Max Q1**	**Max Q2**	**Units**
Drain-Source Voltage		V_{DS}	60	-60	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current	T_C=25°C	I_D	10	-10	A
	T_C=100°C		10	-10	
Pulsed Drain Current		I_{DM}	30	-30	
Continuous Drain Current	T_A=25°C	I_{DSM}	8	-8	A
	T_A=70°C		6.5	-6.5	
Avalanche Current		I_{AS}	14	14	A
Avalanche energy	L=0.1mH	E_{AS}	24	14	mJ
Power Dissipation	T_C=25°C	P_D	12.5	10	W
	T_C=100°C		5	3	
Power Dissipation	T_A=25°C	P_{DSM}	3.5	2.8	W
	T_A=70°C		2.2	1.8	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		°C

Thermal Characteristics							
Parameter		**Symbol**	**Typ Q1**	**Typ Q2**	**Max Q1**	**Max Q2**	**Units**
Maximum Junction-to-Ambient	t ≤ 10s	$R_{\theta JA}$	25	20	35	30	°C/W
Maximum Junction-to-Ambient	Steady-State		50	48	70	65	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	7	3.5	10	4.2	°C/W

Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Avalanche Ratings (Note 1)							
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = 30 V, I_D = 4.5 A	N-CH			93	mJ
I_{AR}	Maximum Drain-Source Avalanche Current		N-CH			4.5	A
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA V_{GS} = 0 V, I_D = –250 μA	N-CH P-CH	60 –60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C I_D = –250 μA, Referenced to 25°C	N-CH P-CH		59 –47		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 48 V, V_{GS} = 0 V V_{DS} = –48 V, V_{GS} = 0 V	N-CH P-CH			1 –1	μA
I_{GSS}	Gate-Body Leakage	V_{GS} = ±20 V, V_{DS} = 0 V V_{GS} = ±20 V, V_{DS} = 0 V	N-CH P-CH			±100 ±100	nA
On Characteristics (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA V_{DS} = V_{GS}, I_D = –250 μA	N-CH P-CH	1 –1	1.6 -1.8	3 –3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C I_D = –250 μA, Referenced to 25°C	N-CH P-CH		–5.6 4		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 4.5 A V_{GS} = 10 V, I_D = 4.5 A, T_J = 125°C V_{GS} = 4.5 V, I_D = 4 A	N-CH		35 49 40	50 64 55	mΩ
		V_{GS} = –10 V, I_D = –3.5 A V_{GS} = –10 V, I_D = –3.5 A, T_J = 125°C V_{GS} = –4.5 V, I_D = –3.1 A	P-CH		64 95 75	100 130 120	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V V_{GS} = –10 V, V_{DS} = –5 V	N-CH P-CH	20 –20			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 4.5 A V_{DS} = –5 V, I_D = –3 5 A	N-CH P-CH		15 10		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	N-CH V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz P-CH V_{DS} = –30 V, V_{GS} = 0 V, f = 1.0 MHz	N-CH P-CH		853 980		pF
C_{oss}	Output Capacitance		N-CH P-CH		60 48		pF
C_{rss}	Reverse Transfer Capacitance		N-CH P-CH		29 35		pF
Switching Characteristics (Note 2)							
$t_{d(on)}$	Turn-On Delay Time	N-CH V_{DD} = 30 V, I_D = 1 A, V_{GS} = 10V, R_{GEN} = 6 Ω P-CH V_{DD} = –30 V, I_D = –1 A, V_{GS} = –10 V, R_{GEN} = 6 Ω	N-CH P-CH		6 9.7		ns
t_r	Turn-On Rise Time		N-CH P-CH		6 5.5		ns
$t_{d(off)}$	Turn-Off Delay Time		N-CH P-CH		19 29		ns
t_f	Turn-Off Fall Time		N-CH P-CH		2.5 6		ns
Q_g	Total Gate Charge	N-CH V_{DS} = 30 V, I_D = 4.5 A, V_{GS} = 10 V P-CH V_{DS} = –30 V, I_D = –3.5 A, V_{GS} = –10V	N-CH P-CH		20 23.7		nC
Q_{gs}	Gate-Source Charge		N-CH P-CH		3 2.1		nC
Q_{gd}	Gate-Drain Charge		N-CH P-CH		4.5 7.2		nC

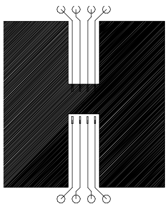
Electrical Characteristics (continued)

T_A = 25°C unless otherwise noted

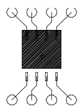
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics and Maximum Ratings							
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-CH P-CH			1.4 –1.4	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.3 A (Note 2) V_{GS} = 0 V, I_S = –1.3 A (Note 2)	N-CH P-CH		0.8 –0.8	1.1 –1.1	V

Notes:

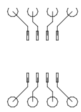
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 0.5 in^2 pad of 2 oz copper



b) 125°C/W when mounted on a .02 in^2 pad of 2 oz copper



c) 135°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

Typical Characteristics: P-CH

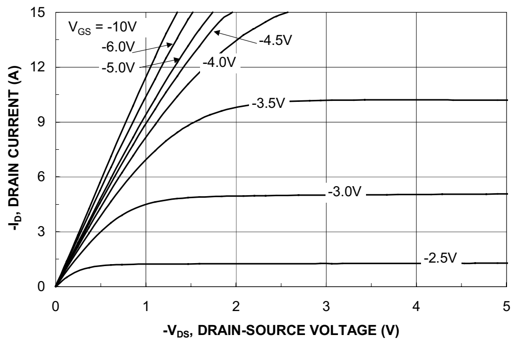


Figure 1. On-Region Characteristics.

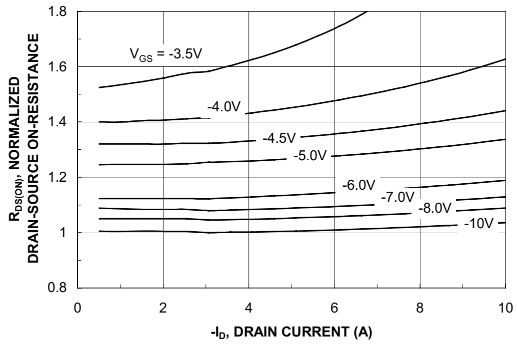


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

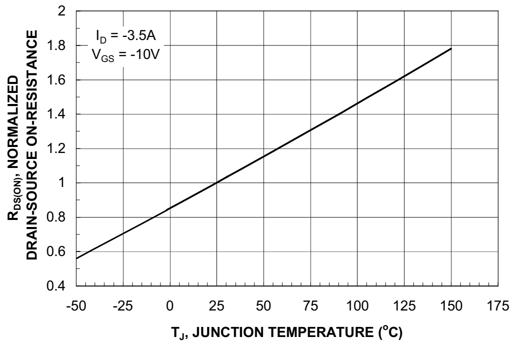


Figure 3. On-Resistance Variation with Temperature.

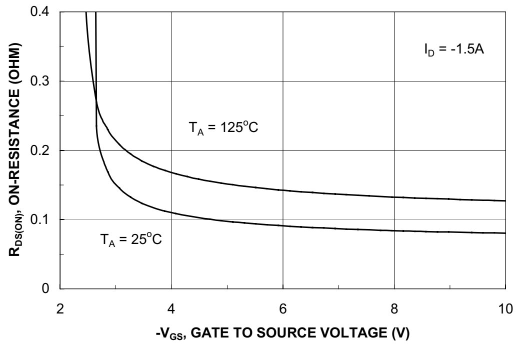


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

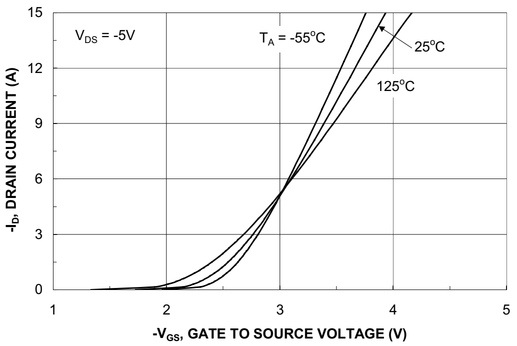


Figure 5. Transfer Characteristics.

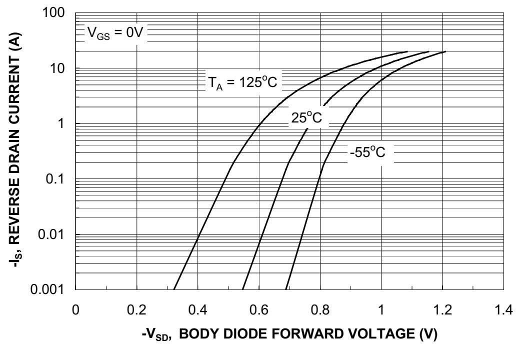


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: P-CH

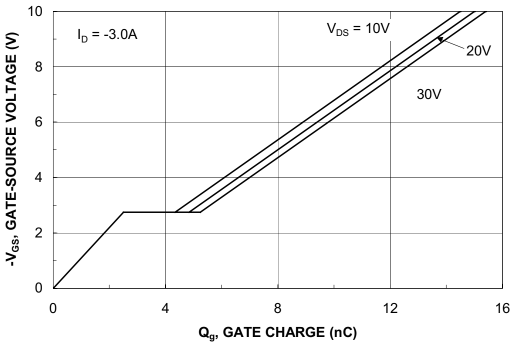


Figure 7. Gate Charge Characteristics.

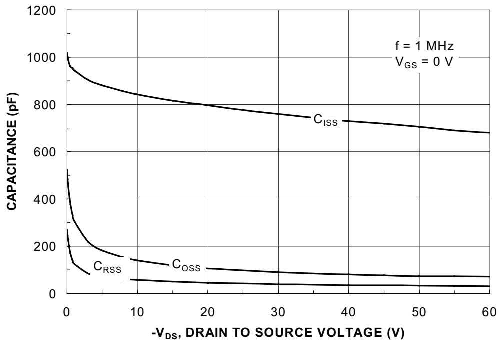


Figure 8. Capacitance Characteristics.

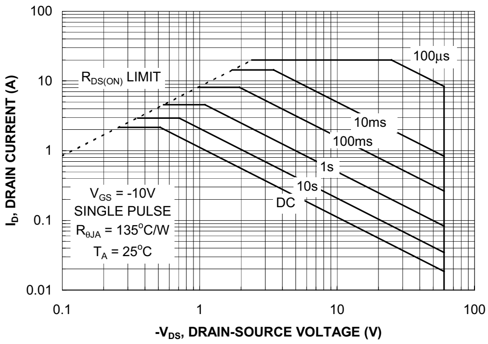


Figure 9. Maximum Safe Operating Area.

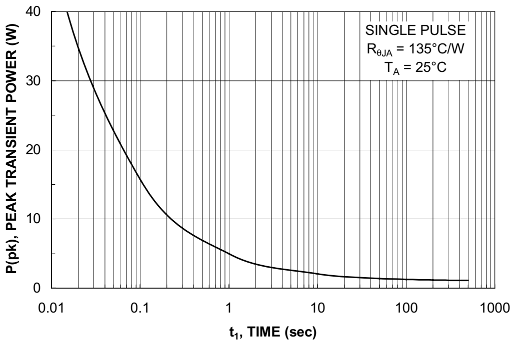


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics: N-CH

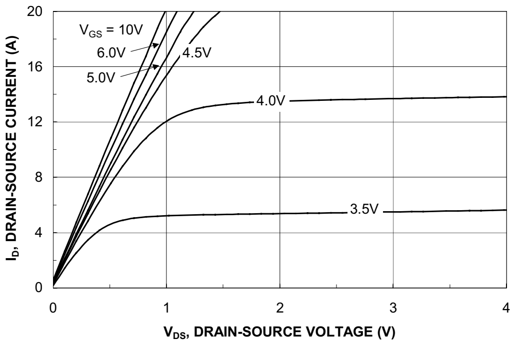


Figure 11. On-Region Characteristics.

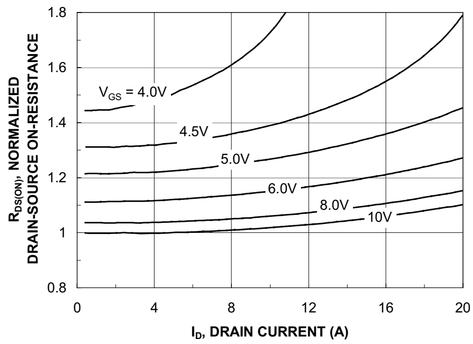


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

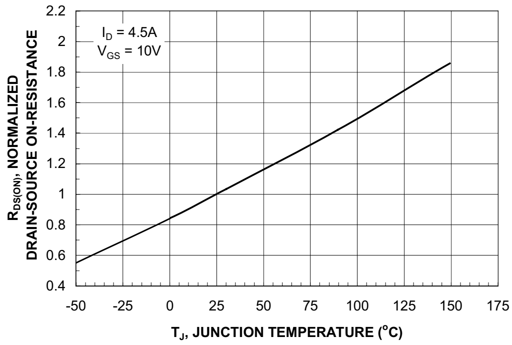


Figure 13. On-Resistance Variation with Temperature.

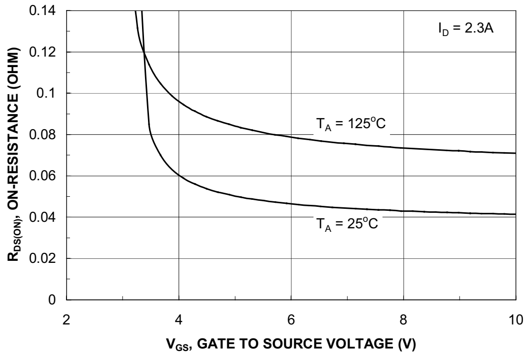


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

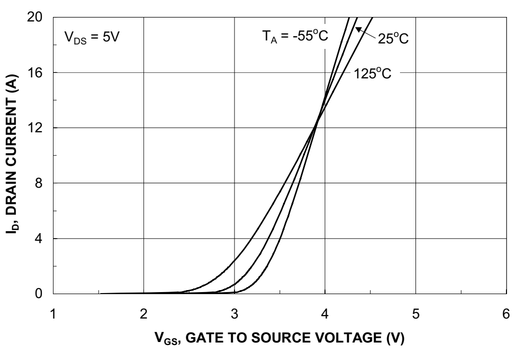


Figure 15. Transfer Characteristics.

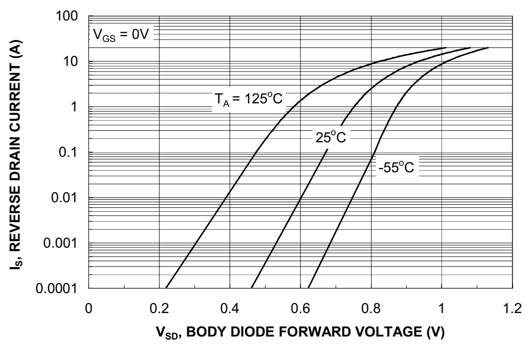


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: N-CH

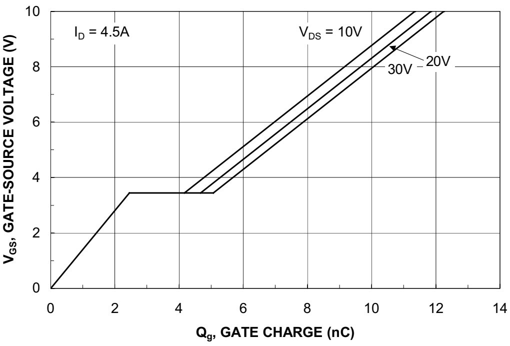


Figure 17. Gate Charge Characteristics.

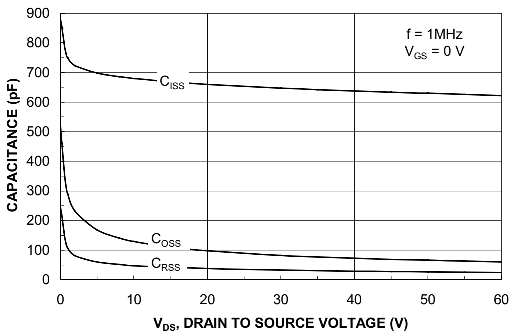


Figure 18. Capacitance Characteristics.

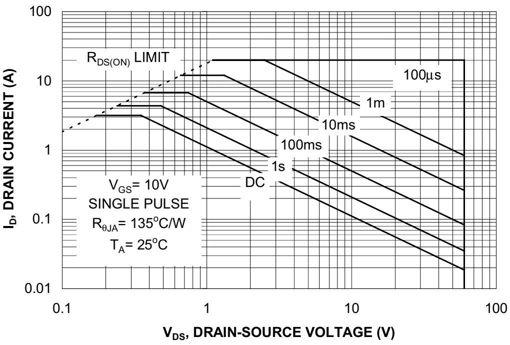


Figure 19. Maximum Safe Operating Area.

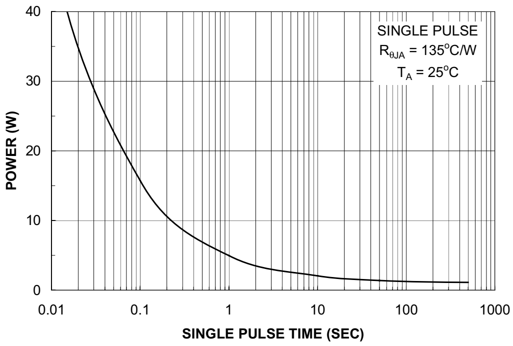


Figure 20. Single Pulse Maximum Power Dissipation.

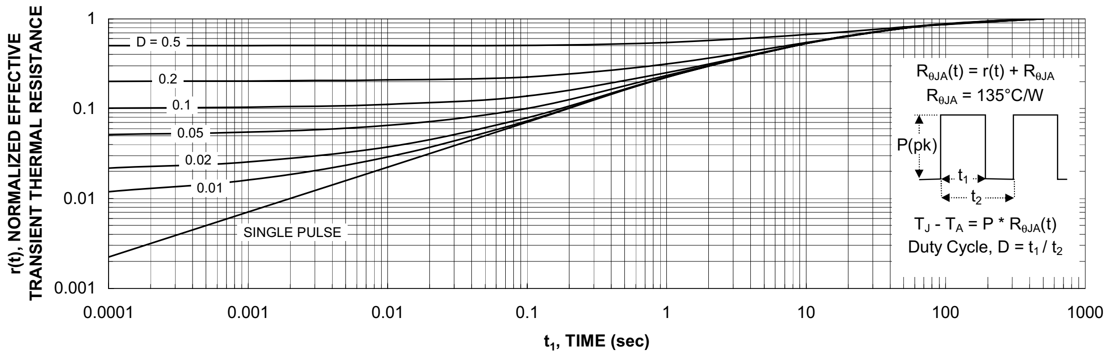
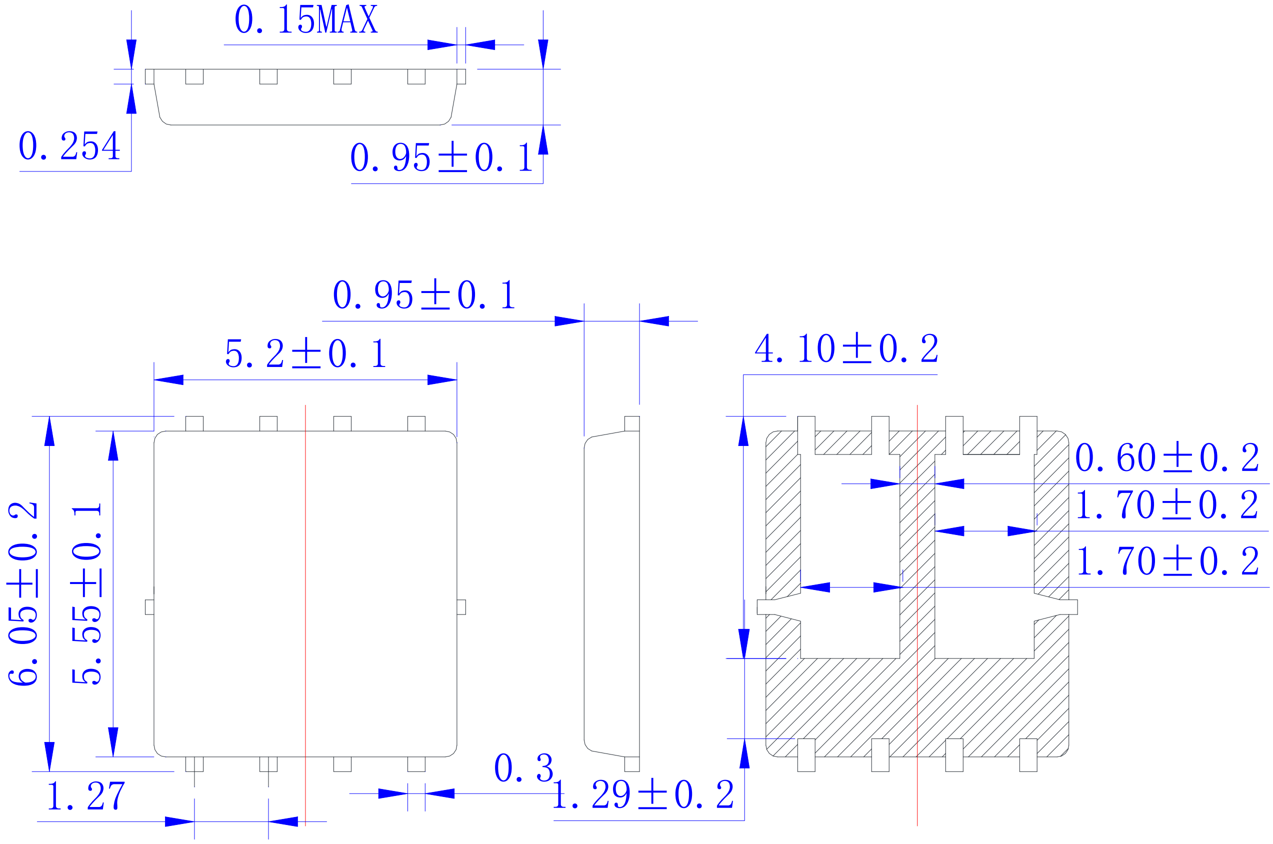


Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

DFN5×6 OUTLINE



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Keep safety first in your circuit designs!

1. MOS-TECH Semiconductor Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.